

MARKO CIRIC

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EDUCATION

University of Toronto | Bachelor of Applied Science, Electrical and Computer Engineering Toronto, ON
Dean's Honours List (2020F, 2021S) 2020-2025

TECHNICAL SKILLS

Hardware: ASIC, FPGA, RTL Design, SystemVerilog, Synopsys VCS, Synopsys Verdi, Lint, Static Timing Analysis, AMD Vivado Design Suite, AMD Vitis Unified Software Platform, Intel Quartus Prime, ModelSim, RDNA, 3D Graphics

Software: C, C++, Python, Perl, Perforce, ARM Assembly

EXPERIENCE

Silicon Design Engineer II • AMD • Full-time August 2025 – Present

- Member of the **Shader Processor Input (SPI) sub-system team** working as an RTL designer in the Graphics pipeline for multiple next generation high-performance Radeon and Instinct (MI series) Graphics Cards.
- Focusing on coordinating shader execution across pipeline stages, managing hardware resource allocation, and optimizing the flow of graphics and compute workloads to maximize parallel processing efficiency.
- Collaborating with design verification team to implement new GPU features and to optimize performance.
- Recipient of the **Q4 2025 Spotlight Award**.

Graphics IP RTL Design Intern • AMD • Co-op May 2023 – August 2024

- Worked on the **Geometry (GE) sub-system team** as an RTL designer in the front-end Graphics pipeline to implement tessellations for multiple next generation high-performance Radeon Graphics Cards.
- Provided day-to-day support for the design team by resolving triage failures using Verdi waveform debugging, resolving Lint errors, and other common debug tasks.
- Implemented performance counters in GE block for improved performance analysis.
- Upgraded common shared modules to be used for standardizing interfaces and implemented the module throughout the GE pipeline.
- Resolved SEC (sequence equivalency checking) failures using static clock timing analysis practices.

TECHNICAL PROJECTS

Optimizing 3D Gaussian Splatting for Qualcomm Snapdragon Hardware September 2024 – April 2025

Completed as my capstone project in a group of 3: ECE496: Design Project

- Implemented and optimized 3D Gaussian Splatting rendering on the Snapdragon 8 Gen 2 SoC.
- Developed a complete rendering pipeline including Gaussian reduction, culling, radix sorting, projection, and display modules.
- Configured touch input to update the camera view; implemented using the Vulkan API to maximize hardware utilization and performance.
- Achieved 20 fps on mobile hardware.

Space Object Detection and Interception System January 2025 – April 2025

Completed as part of a design course in group of 4: ECE532: Digital Systems Design

- Designed a real-time detection and response system for tracking and intercepting space debris.
- Used an array of ultrasonic sensors to detect objects and calculate their trajectories with custom IP blocks in RTL.
- Implemented servo-controlled laser targeting and landing position prediction with HDMI visualization on an Artix-7 FPGA.

Custom Processor Design March 2022 – April 2022

Completed as part of a design course in group of 2: ECE243: Computer Organization

- Designed a 16-bit, 8-register, "ARM-like" processor in Verilog capable of basic instructions, subroutine, stack functionality and with connections to external devices with memory mapped I/O (SWs, KEYS, LEDRs, etc.).
- Simulated and debugged the processor's Verilog using ModelSim to test functionality of the instructions.